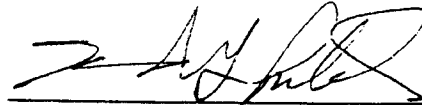


Dated: February 23, 2005

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CERTIFICATE OF SERVICE

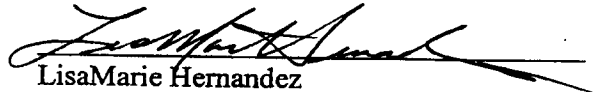
I hereby certify that on this 23rd day of February, 2005, a true and correct copy of the **PLAINTIFF POWER INTEGRATIONS, INC.'S RESPONSES TO DEFENDANTS' FIRST SET OF INTERROGATORIES NOS. 1-28** was caused to be served on the attorneys of record at the following addresses as indicated:

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Exhibit A

**CLAIM CHART COMPARING
THE CLAIMS OF THE BALAKRISHNAN '851 PATENT
WITH THE FAIRCHILD FSD210'¹
(Exhibit A)**

| Claim 1 | |
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| 1. A pulse width modulated switch comprising: | The pulse width modulated switch of the patent is disclosed as element 262. See col. 5, line 14-15. |
| a first terminal; | The first terminal is disclosed as element 300. See col. 5, lines 27-28. |
| a second terminal; | The second terminal is disclosed as element 305. See col. 5, lines 27-28. |
| a switch comprising a control input, said switch allowing a signal to be transmitted between said first terminal and said second terminal according to a drive signal provided at said control input; | <p>Plain meaning of "switch" in this context is a device that allows a signal to pass between two terminals based on the state of a third "control" terminal. An example of such a device is a transistor.</p> <p>Dictionary definitions: "1. a device for making and breaking an electrical connection." Concise Oxford English Dictionary, Tenth Edition, 2002.</p> <p>The specification is consistent with this plain meaning: "Steady-state operation of the pulse width modulated switch 262, i.e. non start up operation, will now be described. PWM oscillator 480 provides pulse width modulation oscillation signal 415 to pulse width modulation comparator 609, the output of which will be high when the magnitude of pulse width modulation signal 415 is greater than the magnitude of a feedback signal 296 which is a function of the input provided at feedback terminal 295. When the output of pulse width modulation comparator 609 is high or-gate 425 is triggered to go high, which in turn resets pulse width modulation latch 430, removing the on signal from the control input of switch 435, thereby turning off switch 435. Pulse width modulation latch 430 is set by clock signal 603, which is provided at the beginning of each cycle of pulse width modulation oscillator 480. Drive circuit 615, which is presently preferred to be an and-gate, receives the output of pulse width modulation latch 430, power up signal 420, and maximum duty cycle signal 607. As long as each one of the signals is high, drive signal 610 is</p> |
| | <p>"The FSD210 is a monolithic high voltage power switching regulator that combines an LDMOS SenseFET with a voltage mode PWM control block." FSD210 Datasheet Rev. 1.0.0 ("Datasheet") at 1</p> <p>"Drain" terminal (pin 7). See Datasheet at 1 (internal block diagram) and 2</p> <p>"Ground/Source" terminal (Pins 1,2,3). See Datasheet at 1 and 2</p> <p>"SenseFET." See Datasheet at 1. The SenseFET is controlled by the signal from the "Driver" and NOR gate. See Datasheet at 1 (internal block diagram).</p> |

¹ PT's analysis related to the FSD210 is representative. Based on the information available to PT, the other accused Fairchild products appear to incorporate identical or substantially identical circuits and, therefore, this analysis is presently believed to apply equally to all accused products.

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| <p>Claim language</p> <p>a frequency variation circuit that provides a frequency variation signal;</p> | <p>provided to the gate of MOSFET 435, which is coupled between first terminal 300 and second terminal 305 of the pulse width modulated switch 262. When any of the output of pulse width modulation latch 430, power up signal 420, or maximum duty cycle signal 607 goes low drive signal 610 is no longer provided and switch 435 ceases conduction." Col. 8, line 46- col. 9, line 3.</p> <p>Plain meaning of "frequency variation circuit" is a structure that provides a signal (the "frequency variation signal") that is used to modulate or change the frequency at which the switch is operated.</p> <p>Dictionary Definitions:</p> <p>"Frequency modulation: the modulation of a radio or other wave by variation of its frequency, especially to carry an audio signal." Concise Oxford English Dictionary, Tenth Edition, 2002.</p> <p>The specification is consistent with this meaning. The specification discloses in detail two possible embodiments of circuits, in the form of low frequency oscillators, that provide the claimed frequency variation signal.</p> <p>"Varying the frequency of operation of the pulse width modulated switch by varying the oscillation frequency of the oscillator is referred to as frequency jitter." Col.3, lines 28-30.</p> <p>"Another object of an aspect of the present invention is directed toward a pulse width modulated switch that has integrated frequency variation capabilities." Col.4, lines 21-23.</p> <p>"Alternatively, or in addition to soft start functionality, pulse width modulated switch 262 may also have frequency jitter functionality. That is, the switching frequency of the pulse width modulated switch 262 varies according to an internal frequency variation signal. This has an advantage over the frequency jitter operation of FIG. 1 in that the frequency range of the presently preferred pulse width modulated switch 262 is known and fixed, and is not subject to the line voltage or load magnitude variations." Col. 6, lines 10-17.</p> <p>"Referring to FIG. 3, frequency variation signal 400 is utilized by the pulse width modulated switch 262 to vary its switching frequency within a frequency range. The frequency variation signal 400 is provided by frequency variation circuit 405, which preferably comprises an oscillator that operates at a lower frequency than main oscillator 465. The frequency variation signal 400, is presently preferred to be a triangular waveform that preferably oscillates between four point five (4.5) volts and one point five (1.5) volts. Although the presently preferred frequency variation signal 400 is a triangular waveform,</p> |
| | <p>"Frequency Modulation" See Datasheet at 1, 9. Figure in Datasheet indicates a digital, step-up, step-down type of modulation.</p> |

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| <p>an oscillator that provides an oscillation signal having a frequency range, said frequency of said oscillation signal varying within said frequency range according to said frequency variation signal, said oscillator further providing a maximum duty cycle signal comprising a first state and a second state; and</p> | <p>alternate frequency variation signals such as ramp signals, counter output signals or other signals that vary in magnitude during a fixed period of time may be utilized as the frequency variation signal." Col. 6, lines 25-38.</p> <p>The detailed implementations are further described in columns 7-11. See also Figs 3, 5, 6 & 9</p> <p>Plain meaning of "oscillator" is a device that provides a repeating periodic signal, i.e. the "oscillation signal." In this case the claimed oscillator signal has a varying frequency. The plain meaning of "maximum duty cycle" signal is a signal that limits the maximum "on-time" of a switch, thereby limiting the maximum duty cycle.</p> <p>Dictionary Definitions: "Oscillator: 1. Apparatus intended to produce or capable of maintaining electric or mechanical oscillations." IEEE Standard Dictionary of Electrical and Electronic Terms, 1993.</p> <p>"Duty cycle: The ratio of the duration (time) that a signal is on to the total period of the signal." Measurement Encyclopedia, National Instruments, http://zone.ni.com</p> <p>The specification is consistent with this plain meaning:</p> <p>"Main oscillator 465 has a current source 470 that is mirrored by mirror current source 475. Main oscillator drive current 615 is provided to the current source input 485 of PWM oscillator 480. The magnitude of the current input into current source input 485 of PWM oscillator 480 determines the frequency of the pulse width modulation oscillation signal 415 which is provided by PWM oscillator 480. In order to vary the frequency of pulse width modulation oscillation signal 415, an additional current source 495 is provided within main oscillator 465. The additional current source 495 is mirrored by additional current source mirror 500. The current provided by additional current source 495 is varied as follows. Frequency variation signal 400 is provided to the gate of main oscillator transistor 505. As the magnitude of frequency variation signal 400 increases so does the voltage at the source of main oscillator transistor 505, due to the increasing voltage at the gate of main oscillator transistor and the relatively constant voltage drop between the gate and source of the main oscillator transistor 505. As the voltage at the source of main oscillator transistor 505 increases so does the current flowing through the main oscillator resistor 510. The current flowing through main oscillator resistor 510 is the same as the current flowing through additional current source 495 which is mirrored by additional current source mirror 500. Since, the presently preferred frequency variation signal 400 is a triangular</p> |
| | <p>The integrated PWM controller features: A fixed oscillator with frequency modulation for reduced EMI." Datasheet at 1.</p> <p>"OSC" See Datasheet at 1 (internal block diagram showing the oscillator having a "frequency modulation" input, a ramp wave output to a PWM comparator and a "clock" output to both a latch and a NOR gate for determining the state of the driver.</p> <p>"Maximum Duty Cycle" See Datasheet at 3 in chart of electrical characteristics showing value for maximum duty cycle. The Datasheet does not explicitly show the max duty cycle signal from the oscillator.</p> |

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| <p>Claim Language</p> | <p>waveform having a fixed period, the magnitude of the current input by additional current source mirror 500 will vary linearly with the magnitude of the rising and falling edges of the frequency variation signal 400. If the frequency variation signal 400 is a ramp signal, the frequency would linearly rise to a peak and then immediately fall to its lowest value. In this way, the current provided to current source input 485 of PWM oscillator 480 is varied in a known fixed range that allows for easy and accurate frequency spread of the high frequency current generated by the pulse width modulated switch. Further, the variance of the frequency is determined by the magnitude of the current provided by additional current source mirror 500, which is in turn a function of the resistance of main oscillation resistor 510." Col. 7, lines 13-53.</p> <p>"Referring to FIG. 5, frequency variation signal 400 which is presently preferred to have a constant period is provided to the main oscillator 465. The magnitude of the pulse width modulator current 615 will approximately be the magnitude of frequency variation signal 400 divided by the resistance of resistor 510 plus the magnitude of the current produced by current source 470. In this way the pulse width modulator current 615 will vary with the magnitude of the frequency variation signal 400. The result is that the frequency of pulse width modulation signal is varied according to the magnitude of this current. It is presently preferred that the pulse width modulator current source produces a constant current having a magnitude of twelve point one (12.1) microamperes, and that frequency variation signal induced current 627 varies between zero (0) and eight hundred (800) nanoamperes. Thereby spreading the frequency of operation of the pulse width modulation oscillator 480 and reducing the average magnitude and the quasi-peak magnitude at all frequency levels of the EMI generated by the power supply." Col. 9, lines 18-36.</p> <p>See also Dmax signal 607 in Figs. 3, 6 & 9.</p> | <p>"Driver" and NOR gate. See Datasheet at 1 (internal block diagram) The state of NOR gate is determined (through latch) by the comparison of the ramp "oscillation signal" and the feedback signal on "Vfb" pin; and also by the state of the "CLK" (i.e. max duty cycle") signal..</p> <p>Plain meaning of "drive circuit" is some structure that generates a signal to determine the state of (i.e. "drive") the switch.</p> <p>Dictionary Definitions:</p> <p>"Driver: (1) (communication practice) An electronic circuit that supplies input to another electronic circuit."</p> <p>The Authoritative Dictionary of IEEE Standards Terms, Seventh Edition.</p> <p>The specification is consistent with this plain meaning:</p> <p>"PWM oscillator 480 provides pulse width modulation oscillation signal 415 to pulse width modulation comparator 609, the output of which will be high when the magnitude of pulse width modulation signal 415 is greater than the magnitude of a feedback signal 296 which is a function of the input</p> |
| <p>a drive circuit that provides said drive signal when said maximum duty cycle signal is in said first state and a magnitude of said oscillation signal is below a variable threshold level.</p> | | |

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| <p>Claim 1</p> | <p>provided at feedback terminal 295." Col. 8, lines 48-54.</p> <p>"When the output of pulse width modulation comparator 609 is high or-gate 425 is triggered to go high, which in turn resets pulse width modulation latch 430, removing the on signal from the control input of switch 435, thereby turning off switch 435. Pulse width modulation latch 430 is set by clock signal 603, which is provided at the beginning of each cycle of pulse width modulation oscillator 480. Drive circuit 615, which is presently preferred to be an and-gate, receives the output of pulse width modulation latch 430, power up signal 420, and maximum duty cycle signal 607. As long as each one of the signals is high, drive signal 610 is provided to the gate of MOSFET 435, which is coupled between first terminal 300 and second terminal 305 of the pulse width modulated switch 262. When any of the output of pulse width modulation latch 430, power up signal 420, or maximum duty cycle signal 607 goes low drive signal 610 is no longer provided and switch 435 ceases conduction." Col. 8, line 54 – Col. 9, line 13.</p> | <p>"The FSD210 is a monolithic high voltage power switching regulator that combines an LDMOS SenseFET with a voltage mode PWM control block." Datasheet at 1</p> |
| <p>Claim 2</p> <p>2. The pulse width modulated switch of claim 1 wherein said first terminal, said second terminal, said switch, said oscillator, said frequency variation circuit and said drive circuit comprise a monolithic device.</p> | <p>"Pulse width modulated switch 262 is presently preferred to be a monolithic device." Col. 9, lines 62-63.</p> | <p>"Internal start up switch and soft start" Datasheet at 1</p> <p>"FSD200/210 has an internal soft start circuit that increases the feedback voltage together with the MOSFET current slowly at start up. The soft start time is 3msec in FSD200/210." Datasheet at 8.</p> |
| <p>Claim 4</p> <p>4. The pulse width modulated switch of claim 1 further comprising a soft start circuit that provides a signal instructing said drive circuit to discontinue said drive signal when said magnitude of said oscillation signal is greater than a magnitude of said frequency variation signal.</p> | <p>"Soft start functionality is termed to be a functionality that reduces the inrush currents at start up." Col. 2, lines 57-58. The specification explains that prior art circuits used an external "soft start capacitor" to achieve this functionality and points out the drawback of this approach. See Col 2, line 58-Col. 3, line 8.</p> <p>"Pulse width modulated switch 262 also may have soft start capabilities. When the device to which the power supply is coupled is switched on, a power up signal is generated within the internal circuitry of pulse width modulated switch 262. The power up signal is used to trigger soft start circuitry that reduces the duty cycle of the switch that operates within the pulse width modulated switch 262 for a predetermined period of time, which is presently preferred to be ten (10) milliseconds. Once soft start operation is completed, pulse width modulated switch 262 operates according to its regular duty cycle." Col. 5, line 66-Col. 6, line 9.</p> | |

“The frequency variation signal 400 is provided to soft start circuit 410. During operation soft start circuit 410 is also provided with pulse width modulation frequency signal 415 and power up signal 420. Soft start enable signal 421 goes high at power up and remains high until oscillator signal 400 reaches its peak value for the first time. Soft start circuit 410 will provide a signal to or-gate 425 to reset latch 430 thereby deactivating conduction by the switch 435, which is presently preferred to be a MOSFET. Soft start circuit 410 will instruct switch 435 to cease conduction when the soft start enable signal 421 is provided and the magnitude of the frequency variation signal 400 is less than the magnitude of pulse width modulation signal 415. In other words, start up circuit 410 will allow the switch 435 to conduct as long as soft start enable signal is high and the magnitude of the pulse width modulation signal 415 is below the magnitude of frequency variation signal 400 as depicted in FIG. 4. In this way, the inrush current at startup will be limited for all cycles of operation, including the first cycle. By limiting the inrush current during all cycles of operation, the maximum current through each of the components of the power supply is reduced and the maximum current rating of each component can be decreased. The reduction in the ratings of the components reduces the cost of the power supply. *Soft start signal 440 will no longer be provided by the frequency variation circuit 405 when the frequency variation signal 400 reaches its peak magnitude.*” Col. 6, lines 39-65.

“Operation of soft start circuit 410 will now be explained. Soft start circuit 410 comprises a soft start latch 450 that at its set input receives the power up signal 420 and its reset input receives the soft start signal 440. Soft start enable signal 421 is provided to one input of soft start and-gate 455 while the other input of soft start and-gate 455 is provided with an output from soft start comparator 460. The output of soft start comparator 460 will be high when the magnitude of frequency variation signal 400 is less than the magnitude of pulse width modulation oscillation signal 415.” Col. 6, line 66-Col. 7, line 8.

“Regulation circuit 850 also may have integrated soft start capabilities. When the device to which the power supply is coupled is switched on, a power up signal is generated within the internal circuitry of regulation circuit 850. A power up signal is used to trigger soft start circuitry that reduces the duty cycle of the switch that operates within the pulse width modulated switch 262 for a predetermined period of time, which is presently preferred to be ten (10) milliseconds. Once soft start operation is completed, regulation circuit 850 operates according to its regular duty cycle. Col. 11, lines 31-42.

“The soft start functionality of the presently preferred regulation circuit 850 of FIG. 9, will shorten the on-time of switch 435 to less than the time of the maximum duty cycle signal 607 as long as the soft start enable signal 421 is

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| <p>Claim 1</p> | <p>provided and the magnitude of frequency variation signal 400 is less than the magnitude of main oscillation signal 415." Col. 11, line 64-Col. 12, line 2.</p> | |
| <p>Claim 7</p> <p>7. The pulse width modulated switch of claim 1 wherein said frequency of said oscillation signal varies within said frequency range with a magnitude of said frequency variation signal.</p> | <p>"Varying the frequency of operation of the pulse width modulated switch by varying the oscillation frequency of the oscillator is referred to as frequency jitter." Col. 3, lines 37-39.</p> <p>"Another object of an aspect of the present invention is directed toward a pulse width modulated switch that has integrated frequency variation capabilities." Col. 4, lines 31-33.</p> <p>"Alternatively, or in addition to soft start functionality, pulse width modulated switch 262 may also have frequency jitter functionality. That is, the switching frequency of the pulse width modulated switch 262 varies according to an internal frequency variation signal. This has an advantage over the frequency jitter operation of FIG. 1 in that the frequency range of the presently preferred pulse width modulated switch 262 is known and fixed, and is not subject to the line voltage or load magnitude variations." Col. 6, lines 18-27.</p> <p>"Although the presently preferred frequency variation signal 400 is a triangular waveform, alternate frequency variation signals such as ramp signals, counter output signals or other signals that vary in magnitude during a fixed period of time may be utilized as the frequency variation signal." Col. 6, lines 34-38.</p> <p>"Referring to FIG. 3, frequency variation signal 400 is utilized by the pulse width modulated switch 262 to vary its switching frequency within a frequency range. The frequency variation signal 400 is provided by frequency variation circuit 405, which preferably comprises an oscillator that operates at a lower frequency than main oscillator 465. The frequency variation signal 400, is presently preferred to be a triangular waveform that preferably oscillates between four point five (4.5) volts and one point five (1.5) volts. Although the presently preferred frequency variation signal 400 is a triangular waveform, alternate frequency variation signals such as ramp signals, counter output signals or other signals that vary in magnitude during a fixed period of time may be utilized as the frequency variation signal." Col. 6, lines 35-48.</p> | <p>See datasheet at 9 showing a graph of the frequency range.</p> |
| <p>Claim 9</p> <p>9. The pulse width modulated switch of claim 1 further comprising:</p> | <p>The pulse width modulated switch of the patent is disclosed as element 262. See col. 5, line 14-15.</p> | <p>See "Typical circuit" diagram at Datasheet p. 6 and "Typical Applications Circuit" at Datasheet p. 10. This claim would be directly infringed by the FSD210 in a power supply application. Fairchild, through at least its datasheet, induces infringement and</p> |

| Claim Language | contributes to infringement by selling the part. |
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| a rectifier comprising a rectifier input and a rectifier output, said rectifier input receiving an AC mains signal and said rectifier output providing a rectified signal; | "Referring to FIG. 2, EMI filter 200 is coupled to an AC mains voltage 205. The AC mains voltage 205 is rectified by rectifier 210." Col. 4, lines 65-68. |
| a power supply capacitor that receives said rectified signal and provides a substantially DC signal; | "The rectified voltage 215 is provided to power supply capacitor 220 which provides a substantially DC voltage 225." Col. 4, line 67 – Col. 5, line 2. |
| a first winding comprising a first terminal and a second terminal, said first winding receiving said substantially DC signal, said second terminal of said first winding coupled to said first terminal of said switch; and | "The first winding is disclosed as the primary winding 230 of transformer 235. The specification discloses that a first terminal of the primary winding receives the substantially DC voltage, and a second terminal of the primary winding is connected to the pulse width modulated switch." See Col. 5, lines 2-13, and Fig. 2. |
| a second winding magnetically coupled to said first winding. | The specification discloses a secondary winding 240 of the transformer 235 that is magnetically coupled to the primary winding 230. See Col. 5, lines 2-13, and Fig. 2. |
| Claim 10 10. The pulse width modulated switch of claim 1 wherein said variable threshold level is a function of a feedback signal received at a feedback terminal of said pulse width modulated switch. | See Datasheet at 1. "Vfb" terminal is the feedback terminal which receives a feedback signal as further shown in the "typical circuit" diagram at p. 6 and Fig. 3 "PWM and feedback circuit" at p. 7. |
| Claim 11 | |
| 11. A regulation circuit comprising: | For at least the reasons stated with reference to the preamble of claim 1, the Fairchild device satisfies the preamble, if it is in fact a claim limitation. |
| a first terminal; | For at least the reasons stated in reference to claim 1, clause 1, the Fairchild device meets this limitation. |
| a second terminal; | For at least the reasons stated in reference to claim 1, clause 2, the Fairchild device meets this limitation. |
| a feedback terminal coupled to | See Datasheet at 1. "Vfb" terminal is the |

| Claim Language | | | | | | | |
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| disable the regulation circuit; | | regulation circuit 850." Col. 10, lines 17-19. "When the voltage across the load 780 reaches the threshold level, current begins to flow through the optocoupler 800 and zener diode 820 that in turn is used to disable the regulation circuit." Col. 10, lines 50-53. | feedback terminal which receives a feedback signal as further shown in the "typical circuit" diagram at p. 6 and Fig. 3 "PWM and feedback circuit" at p. 7. | | | | |
| a switch comprising a control input, said switch allowing a signal to be transmitted between said first terminal and said second terminal according to a drive signal provided at said control input; | | The language of this clause is substantially similar to the language of claim 1, clause 3. | For at least the reasons stated in reference to claim 1, clause 3, the Fairchild device meets this limitation. | | | | |
| a frequency variation circuit that provides a frequency variation signal; | | The language of this clause is substantially similar to the language of claim 1, clause 4. | For at least the reasons stated in reference to claim 1, clause 4, the Fairchild device meets this limitation. | | | | |
| an oscillator that provides an oscillation signal having a frequency range, said frequency of said oscillation signal varying within said frequency range according to said frequency variation signal, said oscillator further providing a maximum duty cycle signal comprising a first state and a second state; and | | The language of this clause is substantially similar to the language of claim 1, clause 5. | For at least the reasons stated in reference to claim 1, clause 5, the Fairchild device meets this limitation. | | | | |
| a drive circuit that provides said drive signal when said maximum duty cycle signal is in said first state and said regulation circuit is not disabled. | | The language of this clause is substantially similar to the language of claim 1, clause 6. | For at least the reasons stated in reference to claim 1, clause 6, the Fairchild device meets this limitation. | | | | |
| Claim 13 | | | | | | | |
| 13. The regulation circuit of claim 11 further comprising a soft start circuit that provides a signal instructing said drive circuit to discontinue said drive signal according to a magnitude of said frequency variation signal. | | The language of this clause is substantially similar to the language of claim 4. | For at least the reasons stated in reference to claim 4, the Fairchild device meets this limitation. | | | | |
| Claim 16 | | | | | | | |
| 16. The regulation circuit of claim | | "The presently preferred regulation circuit 850 preferably comprises a | "The FSD210 is a monolithic high voltage | | | | |

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| <p>11 wherein said first terminal, said second terminal, said switch, said frequency variation circuit, and said drive circuit comprise a monolithic device.</p> | <p>monolithic device." Col. 12, lines 3-4.</p> | <p>power switching regulator that combines an LDMOS SenseFET with a voltage mode PWM control block." Datasheet at 1.</p> |
| <p>Claim 17</p> | <p>17. The regulation circuit of claim 11 further comprising:</p> | <p>For at least the reasons stated with reference to claim 9, the Fairchild device infringes this claim in a power supply application.</p> |
| <p>a rectifier comprising a rectifier input and a rectifier output, said rectifier input receiving an AC mains signal and said rectifier output providing a rectified signal;</p> | <p>The specification discloses a voltage regulation circuit as element 850. See Fig. 8. See Col. 10, lines 17-19.</p> | |
| <p>a power supply capacitor that receives said rectified signal and provides a substantially DC signal;</p> | <p>"Referring to FIG. 8, a power supply comprises a bridge rectifier 710 that rectifies an input AC mains voltage." Col. 9 lines 64-65.</p> | |
| <p>a first winding comprising a first terminal and a second terminal, said first winding receiving said substantially DC signal, said second terminal of said first winding coupled to said first terminal of said switch; and</p> | <p>"Power supply capacitors 720 charge with the rectified AC mains voltage to maintain an input DC voltage 725." Col. 9, lines 65-67.</p> | |
| <p>a second winding magnetically coupled to said first winding.</p> | <p>"An AC mains voltage is input through the EMI filter 700 into bridge rectifier 710 which provides a rectified signal to power supply capacitors 710 that provide input DC voltage 725 to primary winding 740. Regulation circuit 850, which preferably operates at a constant frequency an about constant duty cycle at a given input DC voltage 725, allows current to flow through primary winding 740 during its on state of each switching cycle and acts as open circuit in its off state." Col. 10, lines 24-32.</p> | |
| <p>Claim 18</p> | <p>"Transformer 730 includes a primary winding 740 magnetically coupled to a secondary winding 750." Col. 10, lines 8-10.</p> | |
| <p>18. The regulation circuit of claim 11 further comprising a current limit circuit that provides a signal instructing said drive circuit to discontinue said drive signal when a current received at said first terminal of said regulation circuit is above a threshold level.</p> | <p>"The presently preferred regulation circuit has a current limit feature." Col. 11, lines 7-8.</p> | <p>See Datasheet at 1 ("I_{over}" comparator).</p> |

**CLAIM CHART COMPARING
THE CLAIMS OF THE BALAKRISHNAN '876 PATENT
WITH THE FAIRCHILD FSD210¹
(Exhibit A)**

| Infringement Claim 1 | Support | |
|---|--|---|
| <p>A digital frequency jittering circuit for varying the switching frequency of a power supply, comprising:</p> | <p>Plain meaning of frequency jitter is a change or variation in the frequency of a signal.</p> <p>The specification is consistent with the plain meaning.</p> <p>"Each switched mode power supply typically relies on an oscillator switching at a fixed switching frequency or alternately a variable frequency (such as in ringing choke power supply)." Col. 1, lines 15-18.</p> <p>"The jittering operation smears the switching frequency of the power supply over a wide frequency range and thus spreads energy outside of the bandwidth measured by the EMI measurement equipment." Col. 3, lines 59-62.</p> <p>"FIG. 1 shows a digital frequency jittering circuit 100. The digital frequency jittering circuit 100 has a primary oscillator 110 which provides a clock signal to a counter 140. The primary oscillator 110 typically operates between 100 kHz and 130 kHz. The counter 140 can be a seven bit counter. Each output of counter 140, when clocked by primary oscillator 110 represents a particular time interval. The outputs of the counter 140 are provided to a series of frequency jittering current sources 150. The outputs of the series of frequency jittering current sources 150 are presented to the primary oscillator 110 to vary its frequency, as will be described below." Col. 4, lines 28-39.</p> <p><i>U.S. Patent No. 6,107,851 ('851 patent)</i></p> <p>Varying the frequency of operation of the pulse width modulated switch by varying the oscillation frequency of the oscillator is referred to as frequency jitter. See '851 patent at Col. 3, lines 28-30.</p> | <p>"The FSD210 is a monolithic high voltage power switching regulator that combines an LDMOS SenseFET with a voltage mode PWM control block. The integrated PWM controller features: A fixed oscillator with frequency modulation for reduced EMI." FSD210 Datasheet Rev. 1.0.0 ("Datasheet") at 1.</p> |
| <p>an oscillator for generating a signal having a switching frequency, the oscillator having a control input for varying the switching frequency;</p> | <p>Plain meaning of "oscillator" in this context is a device that generates an oscillating signal having a switching frequency, where the switching frequency of the generated signal can be varied using a control input of the oscillator.</p> <p>Dictionary Definitions:</p> <p>"1. Apparatus intended to produce or capable of maintaining electric or mechanical</p> | <p>"OSC." See Datasheet at 1. The OSC is controlled by a "Frequency Modulation" input. See Datasheet at 1, 9 (internal block diagram). Figure in Datasheet indicates a step-up, step-down type of modulation.</p> |

¹ PI's analysis related to the FSD210 is representative. Based on the information available to PI, the other accused Fairchild products appear to incorporate identical or substantially identical circuits and, therefore, this analysis is presently believed to apply equally to all accused products.

| Infringement | Support | Infringing Party's Contentions |
|---|--|---|
| | <p>oscillations.” IEEE Standard Dictionary of Electrical and Electronic Terms, 1993.</p> <p>The specification is consistent with the plain meaning and refers to this oscillator as the primary oscillator.</p> <p>“The outputs of the series of frequency jittering current sources 150 are presented to the primary oscillator 110 to vary its frequency, as will be described below.” Col. 4, lines 37-39.</p> | |
| <p>a digital to analog converter coupled to the control input for varying the switching frequency; and</p> | <p>Plain meaning of digital to analog converter is a device that converts a digital signal or value to an analog signal or value.</p> <p>Dictionary Definitions: “(1) A device, or group of devices, that converts a numerical input signal or code into an output signal some characteristic of which is proportional to the input.” “(3) A circuit or device whose input is information in digital form and whose output is the same information in analog form. In a hybrid computer, the input is a number sequence (or word) coming from the digital computer, while the output is an analog voltage proportional to the digital number.” IEEE Standard Dictionary of Electrical and Electronic Terms, 1993.</p> <p>The specification describes a digital to analog converter as being implemented using a number of current sources or voltage sources.</p> <p>“[A] digital-to-analog (D-to-A) converter 150, which may be implemented as a series of frequency jittering voltage sources or current sources.” Col. 4, lines 65-66.</p> | <p>“Frequency Modulation” input. See Datasheet at 1, 9 (internal block diagram). Figure in Datasheet indicates a step-up, step-down type of modulation.</p> |
| <p>a counter coupled to the output of the oscillator and to the digital to analog converter, the counter causing the digital to analog converter to adjust the control input and to vary the switching frequency.</p> | <p>Plain meaning of counter is a device that counts, i.e., increments or decrements, at each active edge of a control input.</p> <p>Dictionary Definitions: “(B) an instrument for storing integers, permitting these integers to be increased or decreased sequentially by unity or by an arbitrary integer and capable of being reset to zero or to an arbitrary integer.” IEEE Standard Dictionary of Electrical and Electronic Terms, 1993.</p> <p>The specification also describes a counter.</p> <p>“Counter 140 has a plurality of outputs Q 1 -Q 3 (not shown) which are not used. The remaining outputs Q 4 -Q 7 are connected to a digital-to-analog (D-to-A) converter 150, which may be implemented as a series of frequency jittering voltage sources or current sources.” Col. 4, lines 62-66.</p> | <p>“Frequency Modulation” input. See Datasheet at 1, 9 (internal block diagram). Figure in Datasheet indicates a step-up, step-down type of modulation.</p> |

| Infringement | Support | Conclusion |
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| | <p>"During operation, at every eight clock cycles, the counter output Q 4 on line 155 changes state. Similarly, at every 16 clock cycles, the output Q 5 on line 157 changes state and at every 32 clock cycles, the output Q 6 on line 163 changes state, and every 64 clock cycles, the output Q 7 on line 167 changes state. The entire counting cycle thereafter repeats itself." Col. 5, lines 29-35.</p> | |
| <p>Claim 17 A method for generating a switching frequency in a power conversion system, comprising:</p> | <p>The specification describes "switching frequency as follows: "Each switched mode power supply typically relies on an oscillator switching at a fixed switching frequency or alternately a variable frequency (such as in ringing choke power supply)." Col. 3, lines 59-62.</p> | <p>"The FSD210 is a monolithic high voltage power switching regulator that combines an LDMOS SenseFET with a voltage mode PWM control block. The integrated PWM controller features: A fixed oscillator with frequency modulation for reduced EMI." FSD210 Datasheet Rev. 1.0.0 ("Datasheet") at 1.</p> |
| <p>generating a primary voltage;</p> | <p>Plain meaning of primary voltage is a base or initial voltage.</p> <p>Dictionary Definitions "1: not caused by or based on anything else." Concise Oxford English Dictionary, Tenth Edition, 2002.</p> <p>The specification describes in detail the generation of a primary and secondary currents to control an oscillator's frequency. The specification also states:</p> <p>"The means for varying the frequency may include one or more voltage sources connected to the control input; and a counter connected to the output of the oscillator and to the one or more voltage sources. The oscillator may include a primary voltage source connected to the control input; and a differential switch connected to the primary voltage source." Col. 3, lines 10-15.</p> <p>"The remaining outputs Q 4 -Q 7 are connected to a digital-to-analog (D-to-A) converter 150 , which may be implemented as a series of frequency jittering voltage sources or current sources." Col. 4, lines 63-66.</p> | <p>"Frequency Modulation" input. See Datasheet at 1, 9 (internal block diagram). Figure in Datasheet indicates a step-up, step-down type of modulation.</p> |
| <p>cycling one or more secondary voltage sources to generate a secondary voltage which varies over time; and</p> | <p>Plain meaning of secondary voltage is a subsequent or additional voltage.</p> <p>Plain meaning of cycling is repeating a sequence or a pattern, e.g., a periodic waveform or a repeating sequence of counts. The sequence or pattern need not repeat exactly but it should be substantially similar.</p> <p>Dictionary definitions: "1. a series of events that are regularly repeated in the same order. 2. one complete sequence of changes associated with a recurring phenomenon such as an alternating</p> | <p>"Frequency Modulation" input. See Datasheet at 1, 9 (internal block diagram). Figure in Datasheet indicates a step-up, step-down type of modulation.</p> |

| Infringement | Support | Disputing Content |
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| | <p>current, wave, etc.”</p> <p>Concise Oxford English Dictionary, Tenth Edition, 2002.</p> <p>The specification describes in detail the cycling of current sources but explicitly states that the variation signal may be generated with voltages as well. [see above]</p> | |
| <p>combining the secondary voltage with the primary voltage to be received at a control input of a voltage-controlled oscillator for generating a switching frequency which is varied over time.</p> | <p>Plain meaning of voltage controlled oscillator is an oscillator having a variable frequency of oscillation that is determined by a control voltage.</p> <p>Dictionary definitions:</p> <p>“Voltage-controlled oscillator (VCO): An oscillator whose frequency is a function of the voltage of a control signal.”</p> <p>The Authoritative Dictionary of IEEE Standards Terms, Seventh Edition.</p> <p>The specification describes in detail a current controlled oscillator but explicitly states that the oscillator may be a voltage controlled oscillator being fed a series of varying voltages.</p> <p>“The jittering operation smears the switching frequency of the power supply over a wide frequency range and thus spreads energy outside of the bandwidth measured by the EMI measurement equipment.” Col. 1, lines 15-18. [see also above]</p> | <p>“Frequency Modulation” input. See Datasheet at 1, 9 (internal block diagram). Figure in Datasheet indicates a step-up, step-down type of modulation.</p> |
| <p>Claim 18</p> <p>The method of claim 17 further comprising clocking a counter with the output of the oscillator</p> | <p>“The digital frequency jittering circuit 100 has a primary oscillator 110 which provides a clock signal to a counter 140.” Col. 4, lines 27-29.</p> | <p>“Frequency Modulation” input. See Datasheet at 1, 9 (internal block diagram). Figure in Datasheet indicates a step-up, step-down type of modulation.</p> |
| <p>Claim 19</p> <p>The method of claim 17 wherein the primary voltage is V and each of the secondary voltage sources generates a supplemental voltage lower than V, further comprising passing the supplemental voltage to the voltage-controlled oscillator.</p> | <p>See claim 17.</p> | <p>“Frequency Modulation” input. See Datasheet at 1, 9 (internal block diagram). Figure in Datasheet indicates a step-up, step-down type of modulation.</p> |

**CLAIM CHART COMPARING
THE CLAIMS OF THE EKLUND '075 PATENT
WITH THE FAIRCHILD FSD210¹
(Exhibit A)**

| Claim Language | Support | Infringement Contention |
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| Claim 1 | | |
| 1. A high voltage MOS transistor comprising: | <p>"FIG. 1 is a diagrammatic view of a high voltage MOS transistor of the n-channel type embodying the present invention." Col 2, lines 13-15.</p> <p>See, e.g., "Looking now at FIG. 1, an n-channel type, high voltage MOS transistor, indicated generally by reference numeral 10, is formed on a p-substrate 11 covered by a silicon dioxide layer 12." Col. 2, lines 32-35.</p> <p>See, e.g., "It should be noted that the term "substrate" refers to the physical material on which a microcircuit is fabricated. If a transistor is fabricated on a well of n or p type material within a primary substrate of opposite type material, the well material can be considered a secondary substrate. Similarly, if a transistor is fabricated on an epitaxial layer or epi-island that merely supports and insulates the transistor, the epitaxial layer or epi-island can be considered a secondary substrate." Col. 4, lines 55-63.</p> <p>See, e.g., "A p-substrate 11 is covered by a silicon dioxide layer 12 and insulation layer 18." Col. 3, lines 53-55.</p> <p>See also element 11 in Fig. 1.</p> | <p>The FSD210 features a "700V SenseFET power switch." FSD210 Datasheet Rev. 1.0.0 ("Datasheet") at 1.</p> <p>See, in general, RIGA reverse engineering reports and scanning electron microscope images (SEMs) that will be produced. ("RIGA reports"). The RIGA reports show the high-voltage power switch device of the FSD210 is constructed on a p-type semiconductor substrate.</p> |
| a pair of laterally spaced pockets of semiconductor material of a second conductivity type within the substrate and adjoining the substrate surface, | <p>See, e.g., "Beneath the source contact 14, ... a pocket 21 of n+ material [is] diffused into the p-substrate 11." Col. 2, lines 44-46.</p> <p>See, e.g., "Beneath the drain contact 16, a pocket 24 of n+ material is diffused into the substrate." Col. 2, lines 51-53.</p> <p>See also elements 21 and 24 in Fig. 1.</p> | <p>See RIGA reports which show laterally spaced pockets of n-type material in accordance with this claim element.</p> |
| a source contact connected to one pocket, | <p>See, e.g., "The pocket 21 extends from beneath the source contact to the gate 17." Col. 2, lines 46-47.</p> <p>See also element 14 in Fig. 1.</p> | <p>See RIGA reports which show the source contacts.</p> |

¹ PI's analysis related to the FSD210 is representative. Based on the information available to PI, the other accused Fairchild products appear to incorporate identical or substantially identical circuits and, therefore, this analysis is presently believed to apply equally to all accused products.

| Claim Language | Support | Infringement Contention |
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| a drain contact connected to the other pocket, | See, e.g., "Beneath the drain contact 16, a pocket 24 of n ⁺ material is diffused into the substrate." Col. 2, lines 51-53. | See RIGA reports which show the drain contacts. |
| an extended drain region of the second conductivity type extending laterally each way from the drain contact pocket to surface-adjointing positions, | See also element 16 in Fig. 1. See, e.g., "An extended drain region 26 of n-material is formed by diffusion or ion implantation on top of the p-substrate, and extends from beneath gate 17 to the pocket 24 and a similar distance to the opposite side of the pocket." Col. 2, lines 53-57. | See RIGA reports showing an n-type region of material forming an extended drain region in accordance with this limitation. |
| a surface adjoining layer of material of the first conductivity type on top of an intermediate portion of the extended drain region between the drain contact pocket and the surface-adjointing positions, | See also element 26 in Fig. 1. See, e.g., "A top layer 27 of p- material is provided by ion-implantation through the same mask window as the extended drain region to cover an intermediate portion thereof, while the end portions of the drain region are uncovered to contact the silicon dioxide layer 12. The top layer is either connected to the substrate or left floating." Col. 2, lines 57-62. | See RIGA reports showing a p-type layer of material on the surface of the extended drain region in accordance with this limitation. |
| said top layer of material and said substrate being subject to application of a reverse-bias voltage, | See also element 27 in Fig. 1. Plain meaning of "reverse-bias" in this context is a voltage applied across a rectifying junction with a polarity that provides a high-resistance path. For a P-N junction, this means that the N-type side of the junction is at higher potential than the P-type side. By contrast, forward bias causes the junction to become conductive. See, e.g., "The gate 17 controls by field-effect the current flow thereunder laterally through the p-type material to the n-type material in the extended drain region 26. Further flow through the extended drain region can be controlled by the substrate 11 and the top layer 27, which act as gates providing field-effects for pinching off the extended drain region therebetween." Col. 2, line 64-Col. 3, line 2. | See RIGA reports. The top layer and substrate of the high-voltage device are subject to a reverse-bias voltage in operation of the device. |

| Claim Language | Support | Infringement Contention |
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| <p>an insulating layer on the surface of the substrate and covering at least that portion between the source contact pocket and the nearest surface-adjointing position of the extended drain region, and</p> | <p>See, e.g., "A polysilicon gate 17 is positioned between the source contact and the drain contact at a location where the silicon dioxide layer is very thin so that the gate is slightly offset and insulated from the substrate." Col. 2, lines 37-42.</p> <p>See, e.g., "A top layer 27 of p- material is provided by ion-implantation through the same mask window as the extended drain region to cover an intermediate portion thereof, while the end portions of the drain region are uncovered to contact the silicon dioxide layer 12." Col. 2, lines 57-61.</p> <p>See also element 12 in Fig. 1.</p> <p>Silicon dioxide is a well-known insulator.</p> | <p>See RIGA reports showing a silicon-dioxide insulating layer in accordance with this limitation.</p> |
| <p>a gate electrode on the insulating layer and electrically isolated from the substrate region thereunder which forms a channel laterally between the source contact pocket and the nearest surface-adjointing position of the extended drain region, said gate electrode controlling by field-effect the flow of current thereunder through the channel.</p> | <p>See, e.g., "A polysilicon gate 17 is positioned between the source contact and the drain contact at a location where the silicon dioxide layer is very thin so that the gate is slightly offset and insulated from the substrate." Col. 2, lines 37-42.</p> <p>See, e.g., "The gate 17 controls by field-effect the current flow thereunder laterally through the p-type material to the n-type material in the extended drain region 26. Further flow through the extended drain region can be controlled by the substrate 11 and the top layer 27, which act as gates providing field-effects for pinching off the extended drain region therebetween. Thus, the transistor 10 can be considered as an insulated gate, field-effect transistor (IGFET or MOSFET) connected in series with a double-sided, junction-gate field-effect transistor (JFET)." Col. 2, line 64-Col. 3, line 6.</p> <p>See also element 17 in Fig. 1.</p> | <p>See RIGA reports showing the gate structure of the device in accordance with this limitation of the claim.</p> |
| <p>Claim 5 The high voltage MOS transistor of claim 1 combined on the same chip with a low voltage CMOS implemented device.</p> | <p>See, e.g., "As shown in FIG. 4, low voltage, C-MOS implemented devices 43 and 44 can be combined on the same p-substrate 11 as the high voltage devices 10 and 30, shown in FIG. 3." Col. 4, lines 32-35.</p> | <p>The SenseFET and the control circuitry of the FSD210 meet together meet this limitation.</p> |

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**CLAIM CHART COMPARING
THE CLAIMS OF THE BALAKRISHNAN '366 PATENT
WITH THE FAIRCHILD FSD210
(Exhibit A)¹**

| Claim 1 | The pulse width modulated switch of the patent is disclosed as element 262. See col. 5, line 14-15. | The FSD210 is a monolithic high voltage power switching regulator that combines an LDMOS SenseFET with a voltage mode PWM control block." FSD210 Datasheet Rev. 1.0.0 ("Datasheet") at 1 |
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| a first terminal; | The first terminal is disclosed as element 300. See col. 5, lines 27-28. | "Drain" terminal (pin 7). See Datasheet at 1 (internal block diagram) and 2 |
| a second terminal; | The second terminal is disclosed as element 305. See col. 5, lines 27-28. | "Ground/Source" terminal (Pins 1,2,3). See Datasheet at 1 and 2 |
| a switch comprising a control input, the switch allowing a signal to be transmitted between said first terminal and said second terminal according to a drive signal provided at said control input; | <p>Plain meaning of "switch" in this context is a device that allows a signal to pass between two terminals based on the state of a third "control" terminal. An example of such a device is a transistor.</p> <p>Dictionary definitions:</p> <p>"1. a device for making and breaking an electrical connection." Concise Oxford English Dictionary, Tenth Edition, 2002.</p> <p>The specification is consistent with this plain meaning:</p> <p>"Steady-state operation of the pulse width modulated switch 262, i.e. non start up operation, will now be described. PWM oscillator 480 provides pulse width modulation oscillation signal 415 to pulse width modulation comparator 609, the output of which will be high when the magnitude of pulse width modulation signal 415 is greater than the magnitude of a feedback signal 296 which is a function of the input provided at feedback terminal 295. When the output of pulse width modulation comparator 609 is high or-gate 425 is triggered to go high, which in turn resets pulse width modulation latch 430, removing the on signal from the control input of switch 435, thereby turning off switch 435. Pulse width modulation latch 430 is set by clock signal 603, which is provided at the beginning of each cycle of pulse width modulation oscillator 480. Drive circuit 615, which is presently preferred to be an and-gate, receives the output of pulse width modulation latch 430, power up signal 420, and maximum duty cycle signal</p> | <p>"SenseFET." See Datasheet at 1. The SenseFET is controlled by the signal from the "Driver" and NOR gate. See Datasheet at 1 (internal block diagram).</p> |

¹ PI's analysis related to the FSD210 is representative. Based on the information available to PI, the other accused Fairchild products appear to incorporate identical or substantially identical circuits and, therefore, this analysis is presently believed to apply equally to all accused products.

| | | |
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| <p>an oscillator that provides a maximum duty cycle signal comprising an on-state and an off-state;</p> | <p>607. As long as each one of the signals is high, drive signal 610 is provided to the gate of MOSFET 435, which is coupled between first terminal 300 and second terminal 305 of the pulse width modulated switch 262. When any of the output of pulse width modulation latch 430, power up signal 420, or maximum duty cycle signal 607 goes low drive signal 610 is no longer provided and switch 435 ceases conduction." Col. 8, line 46- col. 9, line 3.</p> <p>Plain meaning of "oscillator" is a device that provides a repeating periodic signal, i.e. the "oscillation signal." In this case the claimed oscillator signal has a varying frequency. The plain meaning of "maximum duty cycle" signal is a signal that limits the maximum "on-time" of a switch, thereby limiting the maximum duty cycle.</p> <p>Dictionary Definitions: "Oscillator: 1. Apparatus intended to produce or capable of maintaining electric or mechanical oscillations." IEEE Standard Dictionary of Electrical and Electronic Terms, 1993.</p> <p>"Duty cycle: The ratio of the duration (time) that a signal is on to the total period of the signal." Measurement Encyclopedia, National Instruments, http://zone.ni.com</p> <p>The specification is consistent with this plain meaning:</p> <p>"Main oscillator 465 has a current source 470 that is mirrored by mirror current source 475. Main oscillator drive current 615 is provided to the current source input 485 of PWM oscillator 480. The magnitude of the current input into current source input 485 of PWM oscillator 480 determines the frequency of the pulse width modulation oscillation signal 415 which is provided by PWM oscillator 480." Col. 7, lines 23-30.</p> <p>See also Dmax signal 607 in Figs. 3, 6 & 9.</p> | <p>"OSC" See Datasheet at 1 (internal block diagram showing the oscillator having a "frequency modulation" input, a ramp wave output to a PWM comparator and a "clock" output to both a latch and a NOR gate for determining the state of the driver.</p> <p>"Maximum Duty Cycle" See Datasheet at 3 in chart of electrical characteristics showing value for maximum duty cycle.</p> |
| <p>a drive circuit that provides said drive signal according to said maximum duty cycle signal; and</p> | <p>Plain meaning of "drive circuit" is some structure that generates a signal to determine the state of (i.e. "drive") the switch..</p> <p>Dictionary Definitions: "Driver: (1) (communication practice) An electronic circuit that supplies input to another electronic circuit." The Authoritative Dictionary of IEEE Standards Terms, Seventh Edition.</p> <p>The specification is consistent with this meaning.</p> <p>"PWM oscillator 480 provides pulse width modulation oscillation signal</p> | <p>"Driver" and NOR gate. See Datasheet at 1 (internal block diagram) The state of NOR gate is determined (through latch) by the comparison of the ramp "oscillation signal" and the feedback signal on "Vfb" pin; and also by the state of the "CLK" (i.e. max duty cycle) signal.</p> |

| Claim Language | | <p>415 to pulse width modulation comparator 609, the output of which will be high when the magnitude of pulse width modulation signal 415 is greater than the magnitude of a feedback signal 296 which is a function of the input provided at feedback terminal 295. When the output of pulse width modulation comparator 609 is high or-gate 425 is triggered to go high, which in turn resets pulse width modulation latch 430, removing the on signal from the control input of switch 435, thereby turning off switch 435. Pulse width modulation latch 430 is set by clock signal 603, which is provided at the beginning of each cycle of pulse width modulation oscillator 480. Drive circuit 615, which is presently preferred to be an and-gate, receives the output of pulse width modulation latch 430, power up signal 420, and maximum duty cycle signal 607. As long as each one of the signals is high, drive signal 610 is provided to the gate of MOSFET 435, which is coupled between first terminal 300 and second terminal 305 of the pulse width modulated switch 262. When any of the output of pulse width modulation latch 430, power up signal 420, or maximum duty cycle signal 607 goes low drive signal 610 is no longer provided and switch 435 ceases conduction." Col. 8, line 48-Col. 9, line 13.</p> | <p>"Soft start functionality is termed to be a functionality that reduces the inrush currents at start up." Col. 2, lines 57-58. The specification explains that prior art circuits used an external "soft start capacitor" to achieve this functionality and points out the drawback of this approach. See Col. 2, line 58-Col. 3, line 8.</p> <p>"Pulse width modulated switch 262 also may have soft start capabilities. When the device to which the power supply is coupled is switched on, a power up signal is generated within the internal circuitry of pulse width modulated switch 262. The power up signal is used to trigger soft start circuitry that reduces the duty cycle of the switch that operates within the pulse width modulated switch 262 for a predetermined period of time, which is presently preferred to be ten (10) milliseconds. Once soft start operation is completed, pulse width modulated switch 262 operates according to its regular duty cycle." Col. 5, line 66-Col. 6, line 9.</p> <p>"The frequency variation signal 400 is provided to soft start circuit 410. During operation soft start circuit 410 is also provided with pulse width modulation frequency signal 415 and power up signal 420. Soft start enable signal 421 goes high at power up and remains high until oscillator signal 400 reaches its peak value for the first time. Soft start circuit 410 will provide a signal to or-gate 425 to reset latch 430 thereby deactivating conduction by the switch 435, which is presently preferred to be a MOSFET. Soft start circuit 410 will instruct switch 435 to cease</p> |
|---|--|---|--|
| <p>a soft start circuit that provides a signal instructing said drive circuit to disable said drive signal during at least a portion of said on-state of said maximum duty cycle.</p> | | | <p>"FSD200/210 has an internal soft start circuit that increases the feedback voltage together with the MOSFET current slowly at start up. The soft start time is 3msec in FSD200/210." Datasheet at 8.</p> |

conduction when the soft start enable signal 421 is provided and the magnitude of the frequency variation signal 400 is less than the magnitude of pulse width modulation signal 415. In other words, start up circuit 410 will allow the switch 435 to conduct as long as soft start enable signal is high and the magnitude of the pulse width modulation signal 415 is below the magnitude of frequency variation signal 400 as depicted in FIG. 4. In this way, the inrush current at startup will be limited for all cycles of operation, including the first cycle. By limiting the inrush current during all cycles of startup operation, the maximum current through each of the components of the power supply is reduced and the maximum current rating of each component can be decreased. The reduction in the ratings of the components reduces the cost of the power supply. Soft start signal 440 will no longer be provided by the frequency variation circuit 405 when the frequency variation signal 400 reaches its peak magnitude." Col. 6, lines 39-65.

"Operation of soft start circuit 410 will now be explained. Soft start circuit 410 comprises a soft start latch 450 that at its set input receives the power up signal 420 and its reset input receives the soft start signal 440. Soft start enable signal 421 is provided to one input of soft start and-gate 455 while the other input of soft start and-gate 455 is provided with an output from soft start comparator 460. The output of soft start comparator 460 will be high when the magnitude of frequency variation signal 400 is less than the magnitude of pulse width modulation oscillation signal 415." Col. 6, line 66-Col. 7, line 8.

"Regulation circuit 850 also may have integrated soft start capabilities. When the device to which the power supply is coupled is switched on, a power up signal is generated within the internal circuitry of regulation circuit 850. A power up signal is used to trigger soft start circuitry that reduces the duty cycle of the switch that operates within the pulse width modulated switch 262 for a predetermined period of time, which is presently preferred to be ten (10) milliseconds. Once soft start operation is completed, regulation circuit 850 operates according to its regular duty cycle. Col. 11, lines 31-42.

"The soft start functionality of the presently preferred regulation circuit 850 of FIG. 9, will shorten the on-time of switch 435 to less than the time of the maximum duty cycle signal 607 as long as the soft start enable signal 421 is provided and the magnitude of frequency variation signal 400 is less than the magnitude of main oscillation signal 415." Col. 11, line 64-Col. 12, line 2.

| Claim Comparison | | |
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| <p>2. The pulse width modulated switch of claim 1 wherein said a first terminal, said second terminal, said switch, said oscillator, said drive circuit and said soft start circuit comprise a monolithic device.</p> | <p>"Pulse width modulated switch 262 is presently preferred to be a monolithic device." Col. 9, lines 62-63.</p> | <p>"The FSD210 is a monolithic high voltage power switching regulator that combines an LDMOS SenseFET with a voltage mode PWM control block." FSD210 Datasheet Rev. 1.0.0 ("Datasheet") at 1</p> |
| <p>Claim 8</p> <p>8. The pulse width modulated switch of claim 1 further comprising:</p> | <p>The pulse width modulated switch of the patent is disclosed as element 262. See col. 5, line 14-15.</p> | <p>See "Typical circuit" diagram at Datasheet p. 6 and "Typical Applications Circuit" at Datasheet p. 10. This claim would be directly infringed by the FSD210 in a power supply application. Fairchild, through at least its datasheet, induces infringement and contributes to infringement by selling the part.</p> |
| <p>a rectifier comprising a rectifier input and a rectifier output, said rectifier input receiving an AC mains signal and said rectifier output providing a rectifier signal;</p> | <p>"Referring to FIG. 2, EMI filter 200 is coupled to an AC mains voltage 205. The AC mains voltage 205 is rectified by rectifier 210." Col. 4, lines 65-68.</p> | |
| <p>a power supply capacitor that receives said rectified signal;</p> | <p>"The rectified voltage 215 is provided to power supply capacitor 220 which provides a substantially DC voltage 225." Col. 4, line 67 – Col. 5, line 2.</p> | |
| <p>a first winding comprising a first terminal and a second terminal, said first winding receiving a substantially DC signal from said power supply capacitor, said second terminal of said first winding coupled to said first terminal of said pulse width modulated switch; and</p> | <p>The first winding is disclosed as the primary winding 230 of transformer 235. The specification discloses that a first terminal of the primary winding receives the substantially DC voltage, and a second terminal of the primary winding is connected to the pulse width modulated switch. See Col. 5, lines 2-13, and Fig. 2.</p> | |
| <p>a second winding magnetically coupled to said first winding, said first winding capable of being coupled to a load.</p> | <p>The specification discloses a secondary winding 240 of the transformer 235 that is magnetically coupled to the primary winding 230. See Col. 5, lines 2-13, and Fig. 2.</p> | |

| Claim 9 | | |
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| 9. A regulation circuit comprising: | The specification discloses a voltage regulation circuit as element 850. See Fig. 8. See Col. 10, lines 17-19. | For at least the reasons stated with reference to the preamble of claim 1, the Fairchild device satisfies the preamble, if it is in fact a claim limitation. |
| a first terminal; | The specification discloses that the voltage regulation circuit has a first terminal. See Fig. 8. | For at least the reasons stated in reference to claim 1, clause 1, the Fairchild device meets this limitation. |
| a second terminal; | The specification discloses that the voltage regulation circuit has a first terminal. See Fig. 8. | For at least the reasons stated in reference to claim 1, clause 2, the Fairchild device meets this limitation. |
| a switch comprising a control input, said switch allowing a signal to be transmitted between said first terminal and said second terminal according to a drive signal provided at said control input; | The language of this clause is substantially similar to the language of claim 1, clause 3. | For at least the reasons stated in reference to claim 1, clause 3, the Fairchild device meets this limitation. |
| a drive circuit that provides said drive signal for a maximum time period of a cycle; and | The language of this clause is substantially similar to the language of claim 1, clause 5. | For at least the reasons stated in reference to claim 1, clause 5, the Fairchild device meets this limitation. |
| a soft start circuit that provides a signal instructing said drive circuit to disable said drive signal during at least a portion of said maximum time period. | The language of this clause is substantially similar to the language of claim 1, clause 6. | For at least the reasons stated in reference to claim 1, clause 6, the Fairchild device meets this limitation. |
| Claim 10 | | |
| 10. The regulation circuit of claim 9 further comprising an oscillator that provides a maximum duty cycle signal to said drive circuit, said maximum duty cycle signal comprising an on-state for said maximum time period. | The language of this clause is substantially similar to the language of claim 1, clause 4. | For at least the reasons stated in reference to claim 1, clause 4, the Fairchild device meets this limitation. |
| Claim 14 | | |
| 14. The regulation circuit | Plain meaning of "frequency variation circuit" is a structure that provides | See datasheet at 9 showing a graph of the |

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| <p>of claim 9 further comprising a frequency variation circuit that provides a frequency variation signal and wherein said maximum time period varies according to a magnitude of said frequency variation signal.</p> | <p>a signal (the "frequency variation signal") that is used to modulate or change the frequency at which the switch is operated.</p> <p>Dictionary Definitions:</p> <p>"Frequency modulation: the modulation of a radio or other wave by variation of its frequency, especially to carry an audio signal." Concise Oxford English Dictionary, Tenth Edition, 2002.</p> <p>The specification is consistent with this meaning. The specification discloses two possible embodiments of circuits, in the form of low frequency oscillators, that provide the claimed frequency variation signal.</p> <p>"Varying the frequency of operation of the pulse width modulated switch by varying the oscillation frequency of the oscillator is referred to as frequency jitter." Col. 3, lines 37-39.</p> <p>"Another object of an aspect of the present invention is directed toward a pulse width modulated switch that has integrated frequency variation capabilities." Col. 4, lines 31-33.</p> <p>"Alternatively, or in addition to soft start functionality, pulse width modulated switch 262 may also have frequency jitter functionality. That is, the switching frequency of the pulse width modulated switch 262 varies according to an internal frequency variation signal. This has an advantage over the frequency jitter operation of FIG. 1 in that the frequency range of the presently preferred pulse width modulated switch 262 is known and fixed, and is not subject to the line voltage or load magnitude variations." Col. 6, lines 18-27.</p> <p>"Although the presently preferred frequency variation signal 400 is a triangular waveform, alternate frequency variation signals such as ramp signals, counter output signals or other signals that vary in magnitude during a fixed period of time may be utilized as the frequency variation signal." Col. 6, lines 34-38.</p> <p>"Referring to FIG. 3, frequency variation signal 400 is utilized by the pulse width modulated switch 262 to vary its switching frequency within a frequency range. The frequency variation signal 400 is provided by frequency variation circuit 405, which preferably comprises an oscillator that operates at a lower frequency than main oscillator 465. The frequency variation signal 400, is presently preferred to be a triangular waveform that preferably oscillates between four point five (4.5) volts and one point five (1.5) volts. Although the presently preferred frequency variation signal 400</p> | <p>frequency range.</p> |
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| Claim 1 | | is a triangular waveform, alternate frequency variation signals such as ramp signals, counter output signals or other signals that vary in magnitude during a fixed period of time may be utilized as the frequency variation signal." Col. 6, lines 35-48. |
| Claim 16 | 16. The regulation circuit of claim 9 wherein said first terminal, said second terminal, said oscillator and said soft start circuit comprise a monolithic device. | "The presently preferred regulation circuit 850 preferably comprises a monolithic device." Col. 12, lines 3-4. |
| Claim 17 | 17. The regulation circuit of claim 16 further comprising a current limit circuit that provides a signal instructing said drive circuit to discontinue said drive signal when a current received at said first terminal of said regulation circuit is above a threshold level. | "The presently preferred regulation circuit has a current limit feature." Col. 11, lines 7-8. |
| Claim 18 | 18. The regulation circuit of claim 9 further comprising a rectifier comprising a rectifier input and a rectifier output, said rectifier input receiving an AC mains signal and said rectifier output providing a rectified signal; | For at least the reasons stated with reference to claim 8, the Fairchild device infringes this claim in a power supply application. |
| | a power supply capacitor that receives said rectified signal; | |
| | a first winding comprising a first terminal and a second terminal, said first winding receiving a substantially DC signal from said power supply | "The FSD210 is a monolithic high voltage power switching regulator that combines an LDMOS SenseFET with a voltage mode PWM control block." Datasheet at 1. |

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| capacitor, said second terminal of said first winding coupled to said first terminal of said regulation circuit; and | and acts as open circuit in its off state." Col. 10, lines 24-32. | |
| a second winding magnetically coupled to said first winding, said first winding capable of being coupled to a load. | "Transformer 730 includes a primary winding 740 magnetically coupled to a secondary winding 750." Col. 10, lines 8-10. | |

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